



2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Christo P. Bojkov, et al.

Docket No.: TI-33887

Serial No.: 10/086,117

Examiner: Lewis, Monica

Filed: 02/26/2002

Art Unit.: 2822

For: Waferlevel Method For Direct Bumping on
Copper Pads In Integrated Circuits

Conf. No.: 2251

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INFORMATION DISCLOSURE STATEMENTAssistant Commissioner For Patents
Alexandria, VA 22313-1450MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)

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Elizabeth Austin

8/15/2003
Date

Dear Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. Copies of the listed references are enclosed.

If required, please charge the fee of \$180 to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

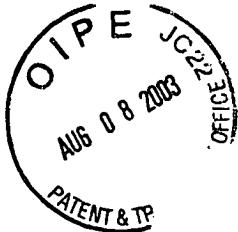
Michael K. Skrehot

Attorney for Applicants

Reg. No. 36,682

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5653

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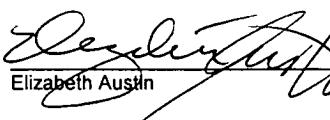
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Substitute for Form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete If Known	
Sheet	1	of	2	Application Number	10/086,117
				Filing Date	02/26/2002
				First Named Inventor	Christo P. Bojkov, et al.
				Group Art Unit	2822
				Examiner Name	Lewis, Monica
				Attorney Docket No.	TI-33887

U.S. PATENT DOCUMENTS					
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)
		Number	Kind Code ² (if known)		
	AA	5,785,236		Cheung, et al.	07/28/1998
	AB	6,213,347 B1		Thomas	04/10/2001
	AC	6,228,680 B1		Thomas	05/08/2001
	AD	6,245,583 B1		Amador, et al.	06/12/2001
	AE	09/775,322		Stierman, et al.	02/01/2001
	AF				
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FOREIGN PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)
		Office ³	Number ⁴	Kind Code ² (if known)		
	BA		JP 1-209746		Moriyama Yoshifumi	23/08/1989
	BB					
	BC					
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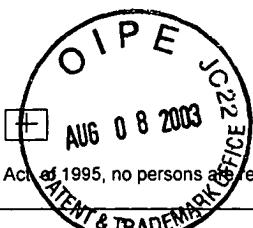
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¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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				First Named Inventor	Christo P. Bojkov, et al.
				Group Art Unit	2822
				Examiner Name	Lewis, Monica
Sheet	2	of	2	Attorney Docket No.	TI-33887

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	"A Silicon and Aluminum Dynamic Memory Technology", Richard A. Larsen, IBM J. Res. Develop., Vol. 24, No. 3, 05/1980, pp. 268-282	
	CB	"Controlled Collapse Reflow Chip Joining", L. F. Miller, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 239-250	
	CC	"Geometric Optimization of Controlled Collapse Interconnections", L. S. Goldman, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 251-265	
	CD	"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Sevgin Oktay, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 272-285	
	CE	"Reliability of Controlled Collapse Interconnections", K. C. Norris and A. H. Landzberg, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 266-271	
	CF	"SLT Device Metallurgy and its Monolithic Extension", P. A. Totta and R. P. Sopher, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 226-238	
	CG	"Studies of the SLT Chip Terminal Metallurgy", B. S. Berry and I. Ames, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 286-296	
	CH		
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